ABSTRACT

An architecture for creating a vertical silicon-on-insulator MOSFET. Generally, an integrated circuit structure includes a semiconductor area with a major surface formed along a plane and a first source/drain contact region formed in the surface. A relatively thin single crystalline layer is oriented vertically above the major surface and comprises a first source/drain doped region over which is located a doped channel region, over which is located a second source/drain region. An insulating layer is disposed adjacent said first and said second source/drain regions and said channel region, serving as the insulating material of the SOI device. In another embodiment, insulating material is adjacent only said first and said second source/drain regions. A conductive region is adjacent the channel region for connecting the back side of the channel region to ground, for example, to prevent the channel region from floating.

In an associated method of manufacturing the semiconductor device, a first source/drain region is formed in a relatively thin vertical layer of single crystalline material. A MOSFET gate region, including a channel and a gate electrode, is formed over the first source/drain region. A second source/drain region is then formed over the channel, the regions being appropriately doped to effect MOSFET action.

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